REMARKS

This is a full and timely response to the outstanding final Office Action mailed December 11, 2007. Through this response, no claims have been amended, canceled, or added. Reconsideration and allowance of the application and pending claims 1-33 are respectfully requested.

I. Claim Rejections - 35 U.S.C. § 103(a)

A. Rejection of Claims 1-27

Claims 1-27 have been rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over *Yan et al.* ("*Yan*," U.S. Pat. No. 6,816,718) in view of *Isberg et al.* ("*Isberg*," U.S. Pat. No. 6,029,052). Applicants respectfully traverse this rejection.

B. Discussion of the Rejection

The M.P.E.P. § 2100-116 states:

> Office policy is to follow *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), in the consideration and determination of obviousness under 35 U.S.C. 103. . . the four factual inquires enunciated therein as a background for determining obviousness are as follows:
>
> (A) Determining the scope and contents of the prior art;
> (B) Ascertaining the differences between the prior art and the claims in issue;
> (C) Resolving the level of ordinary skill in the pertinent art; and
> (D) Evaluating evidence of secondary considerations.

In the present case, it is respectfully submitted that a *prima facie* case for obviousness is not established using the art of record.

Independent Claim 1

Claim 1 recites "wherein...selectively DC-offset correcting comprises selecting...different DC-offset correcting bandwidths based on which system baseband

signal is to be processed." The Office Action states on page 4 that "In implementation, it is implied that the DC correction circuitry will perform a selection or choice in order to determine the amount of adjustment, depending on the baseband signal inputted, needed to provide a common level as discussed in the prior art." However, *Yan* states in column 5, lines 37-42:

> Prior to baseband processing, the differential in-phase and quadrature signals, I+, I-, Q+, and Q- are preferably filtered with filters 50A-50D, respectively, and amplified with amplifiers 52A and 52B to a desired signal level. As illustrated, the relative DC levels for the differential in-phase and quadrature signals, I+, I-, Q+, and Q- are monitored by DC correction circuitry 56. The DC correction circuitry determines the relative DC levels for the differential in-phase and quadrature signals, I+, I-, Q+, and Q- and provides corresponding level adjustment outputs to adjust the DC levels of the individual differential in-phase and quadrature signals I+, I-, Q+, and Q- to effect DC offset correction using summing circuitry 54A-54D. The DC offset correction operates to force the DC levels of the differential in-phase signals I+ and I- to a common level, and the DC levels of the differential quadrature signals Q+ and Q- to a common level to reduce or eliminate distortion caused by having a DC offset between the respective differential signals.

Yan does not teach, disclose, or suggest that the common level to which the DC offset corrector forces the signals has any relationship to the system baseband signal to be processed; rather, the common level appears to be determined relative to the in-phase and quadrature components of a signal after it has been filtered by filters 50A-50D and amplified by amplifiers 52A and 52B. Forcing the signals to a common level in the system of *Yan* would therefore not involve the selection of different DC-offset correcting bandwidths based on which system baseband signal is to be processed as is recited in claim 1.

The Office Action further contends on page 8 that "wherein...selectively DC-offset correcting comprises selecting...different DC-offset correcting bandwidths based on which system baseband signal is to be processed" is disclosed in *Yan*, column 5, lines 22-42, lines 51-57, and column 6, lines 4-12. However, *Yan* states in column 6, lines 39-60:

Next, the control system 32 places an appropriate resistance across the differential input of the dummy LNA 40E based on the communication band for the incoming signal (setp 106) using the load control signal 62. As noted, the selected resistance corresponds to resistance normally seen at the input of the given LAN 40A-40D used during reception of the signal for the given communication band. The control system 32 will then activate the dummy LNA 40E (step 108) and allow the system to settle for a defined period of time (step 110). At this point, any differential output signals of the dummy LNA 40E are likely caused by local oscillator leakage or relatively continuous environmental conditions affecting the differential output signals of the LNAs 40A-40E. These differential output signal of the LNAs 40A-40E result in DC offsets in the differential in-phase and quadrature signals, I+, I-, Q+, and Q- due to the mixing action with the LO signal in the down-conversion circuitry.

Thus the control system 32 activates the DC correction circuitry 56 to monitor the levels of the differential in-phase and quadrature signals I+, I-, Q+, and Q- and provide any necessary DC offset correction (step 110).

Even assuming, *arguendo*, that the system of *Yan* selects a resistance to put across the input dummy LNA based on the communication band of the incoming signal in order to minimize the leakage from the local oscillator in the frequency synthesizer (*Yan*, column 5, lines 16-21), this is not the same as selecting different DC-offset correcting bandwidths based on which system baseband signal is to be processed as is recited in claim 1. The DC-offset circuitry of *Yan* (which is distinct from the dummy LNA) does not appear to be responsive in any way to the ***system baseband signal*** that is ***to be processed***; in column 6, lines 19-22, *Yan* states that the DC correction control signal merely operates to control when the DC correction circuitry operates, not to select different DC-offset correcting bandwidths.

Isberg does not remedy the forgoing deficiencies of *Yan*. Therefore, for at least these reasons, Applicants submit that claim 1 is allowable over the art of record and respectfully request that the rejection of the claim be withdrawn.

Independent Claim 11

Claim 11 recites "bandwidth-switchable DC-offset correction elements." The Office Action states on page 4 that "In implementation, it is implied that the DC

correction circuitry will perform a selection or choice in order to determine the amount of adjustment, depending on the baseband signal inputted, needed to provide a common level as discussed in the prior art." However, *Yan* states in column 5, lines 37-42:

> Prior to baseband processing, the differential in-phase and quadrature signals, I+, I-, Q+, and Q- are preferably filtered with filters 50A-50D, respectively, and amplified with amplifiers 52A and 52B to a desired signal level. As illustrated, the relative DC levels for the differential in-phase and quadrature signals, I+, I-, Q+, and Q- are monitored by DC correction circuitry 56. The DC correction circuitry determines the relative DC levels for the differential in-phase and quadrature signals, I+, I-, Q+, and Q- and provides corresponding level adjustment outputs to adjust the DC levels of the individual differential in-phase and quadrature signals I+, I-, Q+, and Q- to effect DC offset correction using summing circuitry 54A-54D. The DC offset correction operates to force the DC levels of the differential in-phase signals I+ and I- to a common level, and the DC levels of the differential quadrature signals Q+ and Q- to a common level to reduce or eliminate distortion caused by having a DC offset between the respective differential signals.

Yan does not teach, disclose, or suggest that the common level to which the DC offset corrector forces the signals has any bearing on the bandwidth of the DC correction elements; rather, the common level appears to be determined relative to the in-phase and quadrature components of the signal after it has been filtered by filters 50A-50D and amplified by amplifiers 52A and 52B. Forcing the signals to a common level in the system of *Yan* would therefore not teach, disclose, or suggest a bandwidth-switchable DC-offset elements as is recited in claim 11.

The Office Action further contends on page 8 that "wherein...selectively DC-offset correcting comprises selecting...different DC-offset correcting bandwidths based on which system baseband signal is to be processed" is disclosed in *Yan*, column 5, lines 22-42, lines 51-57, and column 6, lines 4-12. However, *Yan* states in column 6, lines 39-60:

> Next, the control system 32 places an appropriate resistance across the differential input of the dummy LNA 40E based on the communication band for the incoming signal (step 106) using the load control signal 62. As noted, the selected resistance corresponds to resistance normally seen at the input of the given LAN 40A-40D used during reception of the signal for the given communication band. The control system 32 will then activate the dummy LNA 40E (step 108) and allow the system to

settle for a defined period of time (step 110). At this point, any differential output signals of the dummy LNA 40E are likely caused by local oscillator leakage or relatively continuous environmental conditions affecting the differential output signals of the LNAs 40A-40E. These differential output signal of the LNAs 40A-40E result in DC offsets in the differential in-phase and quadrature signals, I+, I-, Q+, and Q- due to the mixing action with the LO signal in the down-conversion circuitry.

Thus the control system 32 activates the DC correction circuitry 56 to monitor the levels of the differential in-phase and quadrature signals I+, I-, Q+, and Q- and provide any necessary DC offset correction (step 110).

Even assuming, *arguendo*, that the system of *Yan* selects a resistance to put across the input dummy LNA based on the communication band of the incoming signal in order to minimize the leakage from the local oscillator in the frequency synthesizer (Yan, column 5, lines 16-21), this is not the same as bandwidth-switchable DC-offset correction elements as is recited in claim 11. It is not taught, disclosed, or suggested in *Yan* that the DC-offset element (which is distinct from the dummy LNA) is ***bandwidth-switchable***; in column 6, lines 19-22, *Yan* states that the DC correction control signal merely operates to control when the DC correction circuitry operates, not to switch the bandwidth of the DC-offset correcting elements.

Isberg does not remedy the forgoing deficiencies of *Yan*. Therefore, for at least these reasons, Applicants submit that claim 11 is allowable over the art of record and respectfully request that the rejection of the claim be withdrawn.

Independent Claim 21

Claim 21 recites "means for selecting different DC-offset correcting bandwidths based on which system baseband signal is to be processed." The Office Action states on page 4 that "In implementation, it is implied that the DC correction circuitry will perform a selection or choice in order to determine the amount of adjustment, depending on the baseband signal inputted, needed to provide a common level as discussed in the prior art." However, *Yan* states in column 5, lines 37-42:

Prior to baseband processing, the differential in-phase and quadrature signals, I+, I-, Q+, and Q- are preferably filtered with filters 50A-50D, respectively, and amplified with amplifiers 52A and 52B to a desired signal level. As illustrated, the relative DC levels for the differential in-phase and quadrature signals, I+, I-, Q+, and Q- are monitored by DC correction circuitry 56. The DC correction circuitry determines the relative DC levels for the differential in-phase and quadrature signals, I+, I-, Q+, and Q- and provides corresponding level adjustment outputs to adjust the DC levels of the individual differential in-phase and quadrature signals I+, I-, Q+, and Q- to effect DC offset correction using summing circuitry 54A-54D. The DC offset correction operates to force the DC levels of the differential in-phase signals I+ and I- to a common level, and the DC levels of the differential quadrature signals Q+ and Q- to a common level to reduce or eliminate distortion caused by having a DC offset between the respective differential signals.

Yan does not teach, disclose, or suggest that the common level to which the DC offset corrector forces the signals has any relationship to the system baseband signal to be processed; rather, the common level appears to be determined relative to the in-phase and quadrature components of a signal after it has been filtered by filters 50A-50D and amplified by amplifiers 52A and 52B. Forcing the signals to a common level in the system of *Yan* would therefore not involve the means for selection of different DC-offset correcting bandwidths based on which system baseband signal is to be processed as is recited in claim 21.

The Office Action further contends on page 8 that "wherein...selectively DC-offset correcting comprises selecting...different DC-offset correcting bandwidths based on which system baseband signal is to be processed" is disclosed in *Yan*, column 5, lines 22-42, lines 51-57, and column 6, lines 4-12. However, *Yan* states in column 6, lines 39-60:

Next, the control system 32 places an appropriate resistance across the differential input of the dummy LNA 40E based on the communication band for the incoming signal (setp 106) using the load control signal 62. As noted, the selected resistance corresponds to resistance normally seen at the input of the given LAN 40A-40D used during reception of the signal for the given communication band. The control system 32 will then activate the dummy LNA 40E (step 108) and allow the system to settle for a defined period of time (step 110). At this point, any differential output signals of the dummy LNA 40E are likely caused by local oscillator leakage or relatively continuous environmental conditions affecting the differential output signals of the LNAs 40A-40E. These differential output signal of the LNAs 40A-40E result in DC offsets in

the differential in-phase and quadrature signals, I+, I-, Q+, and Q- due to the mixing action with the LO signal in the down-conversion circuitry.

Thus the control system 32 activates the DC correction circuitry 56 to monitor the levels of the differential in-phase and quadrature signals I+, I-, Q+, and Q- and provide any necessary DC offset correction (step 110).

Even assuming, *arguendo*, that the system of *Yan* selects a resistance to put across the input dummy LNA based on the communication band of the incoming signal in order to minimize the leakage from the local oscillator in the frequency synthesizer (*Yan*, column 5, lines 16-21), this is not the same as means for selecting different DC-offset correcting bandwidths based on which system baseband signal is to be processed as is recited in claim 21. The DC-offset circuitry of *Yan* (which is distinct from the dummy LNA) does not appear to be responsive in any way to the ***system baseband signal*** that is ***to be processed***; in column 6, lines 19-22, *Yan* states that the DC correction control signal merely operates to control when the DC correction circuitry operates, not to select different DC-offset correcting bandwidths.

Isberg does not remedy the forgoing deficiencies of *Yan*. Therefore, for at least these reasons, Applicants submit that claim 21 is allowable over the art of record and respectfully request that the rejection of the claim be withdrawn.

Dependent Claim 2-10, 12-20, 22-27, and 29-33

Because independent claim 1 is allowable over *Yan* in view of *Isberg*, dependent claims 2-10 are allowable as a matter of law for at least the reason that the dependent claims 2-10 contain all elements of their respective base claim. See, e.g., In re Fine, 837 F.2d 1071 (Fed. Cir. 1988). Because independent claim 11 is allowable over *Yan* in view of *Isberg*, dependent claims 12-20 are allowable as a matter of law. Because independent claim 21 is allowable over *Yan* in view of *Isberg*, dependent claims 22-27 are allowable as a matter of law.

Finding of Well Known in Claims 6, 7, 10, 15, 17, and 19

The Office Action states on page 10 that it is well known in the art that filtering can be low pass, all pass, or FIR "since such filters are well known in the art and can be used to perform the functionality of filtering, wherein the filter is chosen based on the inventor's choice and which would produce the output as desired by the inventor". Applicants traverse this finding and submit that such should not be considered well known since the Office Action does not include specific factual findings predicated on sound technical and scientific reasoning to support this conclusion.

Finding of Inherency with regard to Claims 9, 18, and 26

Claim 9 recites, "wherein the processing includes sampling at a first sampling rate for the first baseband signal and a second sampling rate for the second baseband signal." Claim 18 recites, "wherein at least one of the baseband components is configured to sample at a first sampling rate for the first baseband signal and a second sampling rate for the second baseband signal." Claim 26 recites, "wherein the means for processing includes means for sampling at a first sampling rate for the first baseband signal and a second sampling rate for the second baseband signal. The Office Action (p. 11) alleges that since the system of *Yan* comprises one or more DSP elements, and "since I+, I-, Q+, and Q- signals are adjusted based on the mode of the received signal, the signals would be sampled at a rate determined by Nyquist matching the mode of the signal." However, in accordance with In re Robertson, 169 F.3d 743, 745, 49 U.S.P.Q.2d (BNA) 1949, 1950-51 (Fed. Cir. 1999), Applicant traverses these findings as being inadequate to show why the claimed features are necessarily present

in the reference, as *Yan* contains no discussion of different sampling rates for different signals. Consequently, because of the lack of extrinsic evidence required under In re Robertson, the statements in the Office Action are merely conclusory and not adequately supported, and the rejections of claims 9, 18, and 26 are improper.

C. Rejection of Claims 28-33

Claims 28-33 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Peterzell et al.* ("*Peterzell*," U.S. Pat. No. 6,694,129) in view of *Digital Video Broadcasting* (http://www.dvd.org) and further in view of IEEE 802.11a Standards. Applicants respectfully traverse this rejection.

Claim 28 recites: "a direct current (DC)-correction element configured to include switchable bandwidths". The Office Action alleges on page 6 that:

> *Yan* discloses adjusting the LO drive level by varying the gain of the buffer amplifier, which in turn adjust the DC level...The examiner interprets the term "switchable bandwidths" as the bandwidth of the DC offset is switched or adjusted or changed from a current level to a new level. In implementation, the LO drive level is set to one level during a particular procedure and then altered or adjusted when the gain of the amplifier is varied. In the process of altering or adjusting the LO drive level, switching is implied by switching or changing the LO drive level from the current level to a new level.

Applicants assume the use of *Yan* as a reference in the above passage is an error, and that *Peterzell* is the intended reference. The Office Action further alleges on page 14 that the limitation is disclosed in *Peterzell*, column 9, lines 30-35, and column 10, lines 51-55. However, the relevant portion of *Peterzell* states (column 10, lines 51-55):

> However, because the DC output of the LO I and Q channel mixers is related to the LO leakage, varying the LO drive level changes the DC offset. Therefore, the DC offset may need to be removed before baseband signals may be demodulated.

The changes in the DC offset that result from the variations in the LO drive appear to be an undesirable side effect of the variations in the LO drive, as evidenced by the need to remove the DC offset from the baseband signals. However, changes in

the DC offset do not equal changes in the DC offset correction element, and while the DC cancellation module of *Peterzell* is discussed in more detail in column 13, lines 44-column 14, line 10, nowhere does *Peterzell* go into any detail about the bandwidth of the DC correction element that removes the DC offset. The only switchable aspect of the DC cancellation module of *Peterzell* appears to be the speed (column 13, lines 59-61), which is distinct from the bandwidth. Therefore, *Peterzell* does not disclose, teach, or suggest "a direct current (DC)-correction element configured to include switchable bandwidths" as is recited in independent claim 28. Neither *Digital Video Broadcasting* or the IEEE 802.11a Standards remedy this deficiency. Therefore, for at least these reasons, Applicants submit that claim 28 is allowable over the art of record and respectfully request that the rejection of the claim be withdrawn.

Because independent claim 28 is allowable over *Peterzell* in view of *Digital Video Broadcasting* and further in view of IEEE 802.11a Standards, dependent claims 29-33 are allowable as a matter of law for at least the reason that the dependent claims 29-33 contain all elements of their respective base claim.

D. Rejection of Claims 28-33

Claims 28-33 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yan* in view of *Digital Video Broadcasting* (http://www.dvd.org) and further in view of *IEEE 802.11a Standards*. Applicants respectfully traverse this rejection.

Claim 28 recites "a direct current (DC)-correction element configured to include switchable bandwidths". The Office Action alleges on page 4 (regarding claims 1, 11, and 21) that "In implementation, it is implied that the DC correction circuitry will perform a selection or choice in order to determine the amount of adjustment, depending on the

baseband signal inputted, needed to provide a common level as discussed in the prior art." However, *Yan* states in column 5, lines 37-42:

> Prior to baseband processing, the differential in-phase and quadrature signals, I+, I-, Q+, and Q- are preferably filtered with filters 50A-50D, respectively, and amplified with amplifiers 52A and 52B to a desired signal level. As illustrated, the relative DC levels for the differential in-phase and quadrature signals, I+, I-, Q+, and Q- are monitored by DC correction circuitry 56. The DC correction circuitry determines the relative DC levels for the differential in-phase and quadrature signals, I+, I-, Q+, and Q- and provides corresponding level adjustment outputs to adjust the DC levels of the individual differential in-phase and quadrature signals I+, I-, Q+, and Q- to effect DC offset correction using summing circuitry 54A-54D. The DC offset correction operates to force the DC levels of the differential in-phase signals I+ and I- to a common level, and the DC levels of the differential quadrature signals Q+ and Q- to a common level to reduce or eliminate distortion caused by having a DC offset between the respective differential signals.

Yan does not teach, disclose, or suggest that the common level to which the DC offset corrector forces the signals has any bearing on the bandwidth of the DC correction elements; rather, the common level appears to be determined relative to the in-phase and quadrature components of the signal after it has been filtered by filters 50A-50D and amplified by amplifiers 52A and 52B. Forcing the signals to a common level in the system of *Yan* would therefore not teach, disclose, or suggest a direct current (DC)-correction element configured to include switchable bandwidths as is recited in claim 28.

The Office Action further contends on page 8 (regarding claims 1, 11, and 21) that "wherein...selectively DC-offset correcting comprises selecting different DC-offset correcting bandwidths based on which system baseband signal is to be processed" is disclosed in *Yan*, column 5, lines 22-42, lines 51-57, and column 6, lines 4-12. However, *Yan* states in column 6, lines 39-60:

> Next, the control system 32 places an appropriate resistance across the differential input of the dummy LNA 40E based on the communication band for the incoming signal (step 106) using the load control signal 62. As noted, the selected resistance corresponds to resistance normally seen at the input of the given LAN 40A-40D used during reception of the signal for the given communication band. The control system 32 will then activate the dummy LNA 40E (step 108) and allow the system to

settle for a defined period of time (step 110). At this point, any differential output signals of the dummy LNA 40E are likely caused by local oscillator leakage or relatively continuous environmental conditions affecting the differential output signals of the LNAs 40A-40E. These differential output signal of the LNAs 40A-40E result in DC offsets in the differential in-phase and quadrature signals, I+, I-, Q+, and Q- due to the mixing action with the LO signal in the down-conversion circuitry.

Thus the control system 32 activates the DC correction circuitry 56 to monitor the levels of the differential in-phase and quadrature signals I+, I-, Q+, and Q- and provide any necessary DC offset correction (step 110).

Even assuming, *arguendo*, that the system of *Yan* selects a resistance to put across the input dummy LNA based on the communication band of the incoming signal in order to minimize the leakage from the local oscillator in the frequency synthesizer (*Yan*, column 5, lines 16-21), this is not the same as a direct current (DC)-correction element configured to include switchable bandwidths as is recited in claim 28. It is not taught, disclosed, or suggested in *Yan* that the DC-offset element (which is distinct from the dummy LNA) switches bandwidth; in column 6, lines 19-22, *Yan* states that the DC correction control signal merely operates to control when the DC correction circuitry operates, not to switch the bandwidth of the DC-offset correcting elements.

Digital Video Broadcasting further in view of *IEEE 802.11a Standards* does not remedy the forgoing deficiencies of *Yan*. Therefore, for at least these reasons, Applicants submit that claim 28 is allowable over the art of record and respectfully request that the rejection of the claim be withdrawn.

Because independent claim 28 is allowable over *Yan* in view of *Digital Video Broadcasting* further in view of *IEEE 802.11a Standards*, dependent claims 29-33 are allowable as a matter of law for at least the reason that the dependent claims 29-33 contain all elements of their respective base claim.

Finding of Well Known in Claims 29, 31, 32, and 33

The Office Action states on page 17 that it is well known in the art that filtering

can be low pass, all pass, or FIR "since such filters are well known in the art and can be used to perform the functionality of filtering, wherein the filter is chosen based on the inventor's choice and which would produce the output as desired by the inventor". Applicants traverse this finding and submit that such should not be considered well known since the Office Action does not include specific factual findings predicated on sound technical and scientific reasoning to support this conclusion.

CONCLUSION

Applicants respectfully submit that Applicants' pending claims 1-33 are in condition for allowance. Any other statements in the Office Action that are not explicitly addressed herein are not intended to be admitted. In addition, any and all findings of inherency are traversed as not having been shown to be necessarily present. Furthermore, any and all findings of well-known art and official notice, and similarly interpreted statements, should not be considered well known since the Office Action does not include specific factual findings predicated on sound technical and scientific reasoning to support such conclusions. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

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